

Introduction

The AXI External Master Connector (axi_ext_master_conn), lets you connect an AXI master device outside of the embedded system module, using embedded module ports, to the slave interface of an AXI Interconnect IP with no intervening logic. The axi_ext_master_conn IP provides the port connection points necessary to represent the connectivity in the system, plus a set of parameters used to configure the slave interface of the connected AXI Interconnect module.

Features

- A set of ports comprising a standard AXI slave interface, modeled as an I/O interface of the IP, which can be made external using XPS tools. It provide the necessary signals that can be connected to an AXI master device in the top-level system.
- One AXI master bus-interface that connects to an AXI Interconnect in the embedded system.
- Directly connects the external slave interface ports to the AXI master bus-interface, and contains no logic or storage.

| LogiCORE IP Facts Table | | | | | |
|--|------------------------|-----|------------|------------|------------|
| Core Specifics | | | | | |
| Core Name | axi_ext_master_conn | | | | |
| Supported Device Family ⁽¹⁾ | Virtex®-6, Spartan®-6, | | | | |
| Supported User Interfaces | AXI4, AXI4-Lite | | | | |
| TBD | Resources | | | | Frequency |
| Configuration | LUTs | FFs | DSP Slices | Block RAMs | Max. Freq. |
| Config1 | 0 | 0 | 0 | 0 | N/A |
| Provided with Core | | | | | |
| Documentation | Product Specification | | | | |
| Design Files | Verilog, VHDL | | | | |
| Example Design | Not Provided | | | | |
| Test Bench | Not Provided | | | | |
| Constraints File | Not Provided | | | | |
| Simulation Model | Verilog, VHDL | | | | |
| Tested Design Tools | | | | | |
| Design Entry Tools | EDK, XPS | | | | |
| Simulation | N/A | | | | |
| Synthesis Tools | XPS | | | | |
| Support | | | | | |
| Provided by Xilinx, Inc. | | | | | |

1. For a complete listing of supported devices, see the [release notes](#) for this core.

Feature Description

The following figure illustrates the AXI external master connection to an AXI Interconnect.

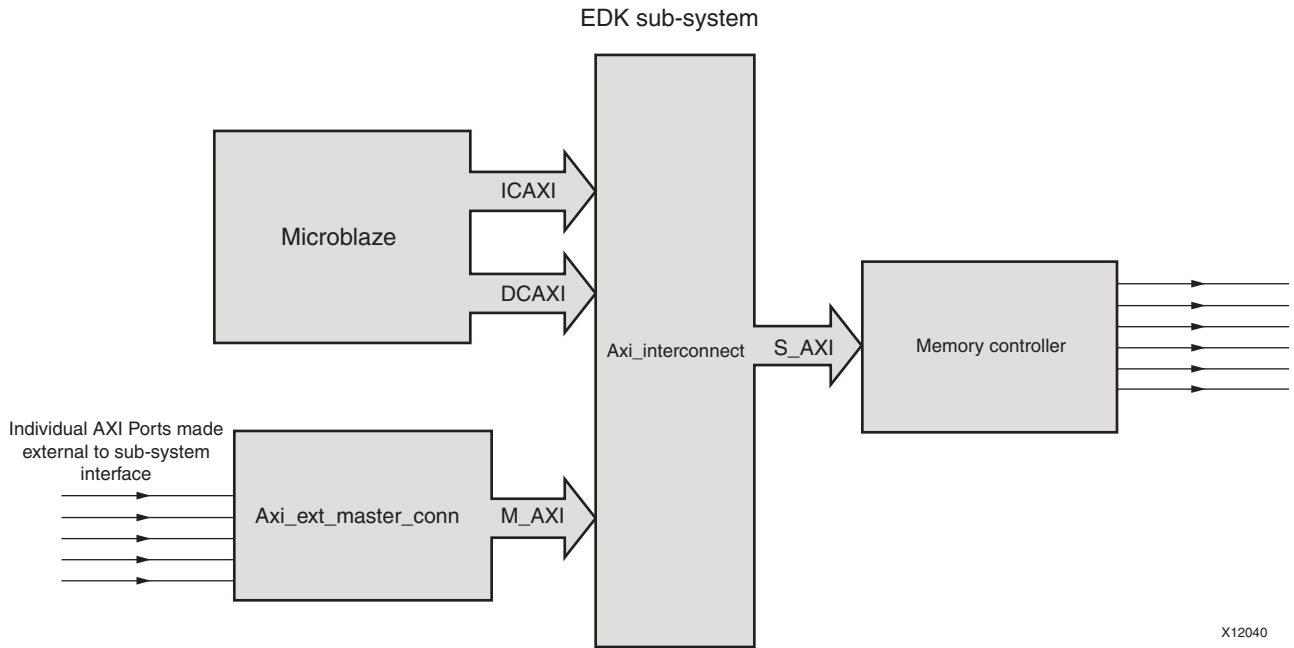


Figure 1: System Using AXI External Master Connector

I/O Signals

The following tables list the external slave signals and master I/O signals.

External Slave Signals

Table 1 lists the external AXI slave interface signals that can connect to embedded system ports.

Table 1: I/O Slave Signals

| Signal Name | Interface | Signal Type | Description |
|---|-----------|-------------|--|
| AXI Write Address Channel Signals (AW) | | | |
| S_AXI_AWLEN [7:0] | AW | I | AXI address Write burst length. |
| S_AXI_AWSIZE [2:0] | AW | I | AXI address Write burst size. |
| S_AXI_AWBURST [1:0] | AW | I | AXI address Write burst type. |
| S_AXI_AWLOCK | AW | I | AXI Write address lock signal. ⁽¹⁾ |
| S_AXI_AWCACHE [3:0] | AW | I | AXI Write address cache control signal. |
| S_AXI_AWPROT [2:0] | AW | I | AXI Write address protection signal. |
| S_AXI_AWQOS [3:0] | AW | I | Channel Quality of Service (QoS). ⁽¹⁾ |
| S_AXI_AWUSER [C_M_AXI_AWUSER_WIDTH-1:0] | AW | I | User-defined AW Channel signals. |
| S_AXI_AWVALID | AW | I | AXI Write address valid. |

1. Advanced signal available for connection only when C_USE_ADVANCED_PORTS=1.

Table 1: I/O Slave Signals (Cont'd)

| Signal Name | Interface | Signal Type | Description |
|---|-----------|-------------|---|
| S_AXI_AWREADY | AW | O | AXI Write address ready. |
| AXI Write Data Channel Signals (W) | | | |
| S_AXI_WDATA [C_M_AXI_DATA_WIDTH-1:0] | W | I | AXI Write data. |
| S_AXI_WSTRB [C_M_AXI_DATA_WIDTH/8-1:0] | W | I | AXI Write data strobes. |
| S_AXI_WLAST | W | I | AXI Write data last signal. Indicates the last transfer in a Write burst. |
| S_AXI_WUSER [C_M_AXI_WUSER_WIDTH-1:0] | W | I | User-defined W Channel signals. |
| S_AXI_WVALID | W | I | AXI Write data valid. |
| S_AXI_WREADY | W | O | AXI Write data Ready. |
| AXI Write Response Channel Signals (B) | | | |
| S_AXI_BID [C_M_AXI_THREAD_ID_WIDTH-1:0] | B | O | AXI Write response ID. ⁽¹⁾ |
| S_AXI_BRESP [1:0] | B | O | AXI Write response code. |
| S_AXI_BUSER | B | O | User defined B channel signals. |
| S_AXI_BVALID | B | O | AXI Write response valid. |
| S_AXI_BREADY | B | I | Write response Ready. |
| AXI Read Address Channel Signals (AR) | | | |
| S_AXI_ARID [C_M_AXI_THREAD_ID_WIDTH-1:0] | AR | I | AXI address Read ID. ⁽¹⁾ |
| S_AXI_ARADDR [C_M_AXI_ADDR_WIDTH-1:0] | AR | I | AXI Read address. |
| S_AXI_ARLEN [7:0] | AR | I | AXI address Read burst length. |
| S_AXI_ARSIZE [2:0] | AR | I | AXI address Read burst size. |
| S_AXI_ARBURST [1:0] | AR | I | AXI address Read burst type. |
| S_AXI_ARLOCK | AR | I | AXI Read address lock signal. ⁽¹⁾ |
| S_AXI_ARCACHE [3:0] | AR | I | AXI Read address cache control signal. |
| S_AXI_ARPROT [2:0] | AR | I | AXI Read address protection signal. |
| S_AXI_ARQOS [3:0] | AR | I | Channel Quality of Service (QoS). ⁽¹⁾ |
| S_AXI_ARUSER [C_S_AXI_ARUSER_WIDTH-1:0] | AR | I | User-defined AR Channel signals. |
| S_AXI_ARVALID | AR | I | AXI Read address valid. |
| S_AXI_ARREADY | AR | O | AXI Read address ready. |
| AXI Read Data Channel Signals (R) | | | |
| S_AXI_RID [C_M_AXI_THREAD_ID_WIDTH-1:0] | R | O | AXI Read data response ID. ⁽¹⁾ |
| S_AXI_RDATA [C_S_AXI_DATA_WIDTH-1:0] | R | O | AXI Read data. |
| S_AXI_RRESP [1:0] | R | O | AXI Read response code. |

1. Advanced signal available for connection only when C_USE_ADVANCED_PORTS=1.

Table 1: I/O Slave Signals (Cont'd)

| Signal Name | Interface | Signal Type | Description |
|---------------------------------------|-----------|-------------|---------------------------------|
| S_AXI_RLAST | R | O | AXI Read data last signal. |
| S_AXI_RUSER [C_S_AXI_RUSER_WIDTH-1:0] | R | O | User-defined R Channel signals. |
| S_AXI_RVALID | R | O | AXI Read valid. |
| S_AXI_RREADY | R | I | Read ready. |

1. Advanced signal available for connection only when C_USE_ADVANCED_PORTS=1.

AXI Master Interface Signals

Table 2 lists the master interface signals that can connect to an AXI Interconnect IP in an embedded system.

Table 2: AXI Master Interface Signals

| Signal Name | Interface | Signal Type | Description |
|---|-----------|-------------|---|
| AXI Write Address Channel Signals (AW) | | | |
| M_AXI_AWID [C_M_AXI_THREAD_ID_WIDTH-1:0] | AW | O | AXI address Write ID. |
| M_AXI_AWADDR [C_M_AXI_ADDR_WIDTH-1:0] | AW | O | AXI Write address. |
| M_AXI_AWLEN [7:0] | AW | O | AXI address Write burst length. |
| M_AXI_AWSIZE [2:0] | AW | O | AXI address Write burst size. |
| M_AXI_AWBURST [1:0] | AW | O | AXI address Write burst type. |
| M_AXI_AWLOCK | AW | O | AXI Write address lock signal. |
| M_AXI_AWCACHE [3:0] | AW | O | AXI Write address cache control signal. |
| M_AXI_AWPROT [2:0] | AW | O | AXI Write address protection signal. |
| M_AXI_AWQOS [3:0] | AW | O | Channel Quality of Service (QoS). |
| M_AXI_AWUSER [C_M_AXI_AWUSER_WIDTH-1:0] | AW | O | User-defined AW Channel signals. |
| M_AXI_AWVALID | AW | O | AXI Write address valid. |
| M_AXI_AWREADY | AW | I | AXI Write address ready. |
| AXI Write Data Channel Signals (W) | | | |
| M_AXI_WDATA [C_M_AXI_DATA_WIDTH-1:0] | W | O | AXI Write data. |
| M_AXI_WSTRB [C_M_AXI_DATA_WIDTH/8-1:0] | W | O | AXI Write data strobes. |
| M_AXI_WLAST | W | O | AXI Write data last signal. Indicates the last transfer in a Write burst. |
| M_AXI_WUSER [C_M_AXI_WUSER_WIDTH-1:0] | W | O | User-defined W Channel signals. |
| M_AXI_WVALID | W | O | AXI Write data valid. |
| M_AXI_WREADY | W | I | AXI Write data ready. |

Table 2: AXI Master Interface Signals (Cont'd)

| Signal Name | Interface | Signal Type | Description |
|---|-----------|-------------|--|
| AXI Write Response Channel Signals (B) | | | |
| M_AXI_BID [C_M_AXI_THREAD_ID_WIDTH-1:0] | B | I | AXI Write response ID. |
| M_AXI_BRESP [1:0] | B | I | AXI Write response code. |
| M_AXI_BUSER | B | I | User-defined B Channel signals. |
| M_AXI_BVALID | B | O | AXI Write response valid. |
| M_AXI_BREADY | B | I | Write response ready. |
| AXI Read Address Channel Signals (AR) | | | |
| M_AXI_ARID [C_S_AXI_ID_WIDTH-1:0] | AR | O | AXI address read ID. |
| M_AXI_ARADDR [C_S_AXI_ADDR_WIDTH-1:0] | AR | O | AXI read address. |
| M_AXI_ARLEN [7:0] | AR | O | AXI address read burst length. |
| M_AXI_ARSIZE [2:0] | AR | O | AXI address read burst size. |
| M_AXI_ARBURST [1:0] | AR | O | AXI address read burst type. |
| M_AXI_ARLOCK | AR | O | AXI read address lock signal. |
| M_AXI_ARCACHE [3:0] | AR | O | AXI read address cache control signal. |
| M_AXI_ARPROT [2:0] | AR | O | AXI read address protection signal. |
| M_AXI_ARQOS [3:0] | AR | O | AR Channel Quality of Service (QoS). |
| M_AXI_ARUSER [C_S_AXI_ARUSER_WIDTH-1:0] | AR | I | User-defined AR Channel signals. |
| M_AXI_ARVALID | AR | O | AXI read address valid. |
| M_AXI_ARREADY | AR | I | AXI read address ready. |
| AXI Read Data Channel Signals (R) | | | |
| M_AXI_RID [C_S_AXI_ID_WIDTH-1:0] | R | I | AXI read data response ID. |
| M_AXI_RDATA [C_S_AXI_DATA_WIDTH-1:0] | R | I | AXI Read data. |
| M_AXI_RRESP [1:0] | R | I | AXI Read response code. |
| M_AXI_RLAST | R | I | AXI read data last signal. |
| M_AXI_RUSER [C_S_AXI_RUSER_WIDTH-1:0] | R | I | User-defined R Channel signals. |
| M_AXI_RVALID | R | I | AXI read valid. |
| M_AXI_RREADY | R | O | Read ready. |

Global I/O Signals

Table 3 lists global signals of the IP.

Table 3: Global I/O Signals

| Signal Name | Interface | Signal Type | Init Status | Description |
|-----------------------|-----------|-------------|-------------|-----------------------|
| Global Signals | | | | |
| ACLK | Global | I | | AXI Bus Clock. |
| ARESETN | Global | I | | AXI active-Low reset. |

Parameters

Table 4 lists the user-visible parameters. In addition to the parameters listed in this table, there are also inferred parameters for the M_AXI interface in the EDK tools. Through the design, these inferred parameters control the behavior of the AXI Interconnect. For a complete list of the interconnect settings related to the AXI interface, see the [AXI Interconnect IP Data Sheet](#) (DS768).

Table 4: External Master Parameters

| Parameter Name | Default Value | Allowable Values | Description |
|-------------------------------|---------------|----------------------------------|---|
| C_USE_ADVANCED_PORTS | 0 | 0, 1 | Controls whether the less-common (advanced) AXI signals are included in the external slave interface. |
| C_M_AXI_PROTOCOL | AXI4 | String (AXI3, AXI4, AXI4LITE) | AXI protocol used by the connected external master device. |
| C_M_AXI_ADDR_WIDTH | 32 | constant (32) | Width of ADDR signals (both S and M interfaces). |
| C_M_AXI_DATA_WIDTH | 32 | Integer (32, 64, 128, 256) | Specifies the width of the WDATA and RDATA signals used by the connected external master device (applies to both S and M interfaces). |
| C_M_AXI_SUPPORTS_READ | 1 | 0,1 | Specifies whether the connected external master device performs reads. |
| C_M_AXI_SUPPORTS_WRITE | 1 | 0,1 | Specifies whether the connected external master device performs Writes. |
| C_M_AXI_SUPPORTS_THREADS | 0 | 0,1 | Specifies whether the connected external master device produces any ID signals (has reordering depth > 1). |
| C_M_AXI_THREAD_ID_WIDTH | 1 | 1-16 | Specifies the number of ID bits produced by the connected external master device. |
| C_M_AXI_SUPPORTS_NARROW_BURST | 1 | 0,1 | Specifies whether the connected external master device produces “narrow bursts” (transfer SIZE less than data width for any multi-beat bursts). |
| C_M_AXI_SUPPORTS_USER_SIGNALS | 0 | 0,1 | Specifies whether the connected external master device has any USER signals on any AXI channels. |
| C_M_AXI_AWUSER_WIDTH | 1 | Integer (1-2147483647) | Specifies the number of AWUSER bits on the connected external master device. |
| C_M_AXI_BUSER_WIDTH | 1 | Integer (1-2147483647) | Specifies the number of BUSER bits on the connected external master device. |

Table 4: External Master Parameters (Cont'd)

| Parameter Name | Default Value | Allowable Values | Description |
|----------------------|---------------|---------------------------|--|
| C_M_AXI_ARUSER_WIDTH | 1 | Integer (1-2147483647) | Specifies the number of ARUSER bits on the connected external master device. |
| C_M_AXI_WUSER_WIDTH | 1 | Integer (1-2147483647) | Specifies the number of WUSER bits on the connected external master device. |
| C_M_AXI_RUSER_WIDTH | 1 | Integer (1-2147483647) | Specifies the number of RUSER bits on the connected external master device. |

Support

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Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|------------|---------|--------------------------|
| 09/21/2010 | 1.00 | Initial Xilinx release. |

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